AAKANKSHA DEVRARI

Assistant Professor in Women Institute of Technology, Campus Institute of Veer Madho Singh Bhandari Uttarakhand Technical University Dehradun, Uttarakhand (Sep 2023 - present) with total 6 years of experience.

Ph.D. status: Thesis submitted in July 2023, University of Petroleum & Energy Studies, Dehradun

Tel: **+91- 7060111700(M)** E-mail: **aks.uit08@gmail.com**

Thesis Title: "FPGA Performance Analysis of Different Forward Error Correction Codes for 5G Communication System".

Objective
My career goal is to become expertise in field where I am working and constantly update myself with the latest technologies to move up in ladder & contribute to the growth of organization.

Academic Qualification	
High school	ST. Theresa's, Srinagar Garhwal , Uttarakhand, 2005, 70%
Intermediate	ST. Theresa's, Srinagar Garhwal , Uttarakhand, 2007, 72%

Professional Qualification	
Master of Technology (VLSI)	Faculty of Technology, Uttarakhand Technical University, Dehradun, Uttarakhand, (2011-2013) 82.3%
Bachelor of Technology (Electronics & Comm.)	Uttaranchal Institute of Technology, Uttarakhand Technical University, Dehradun, Uttarakhand, (2007-2011) 74%

Experience

- 3 years of experience as a Doctoral research Fellow, R&D Department, University of Petroleum & Energy Studies, Dehradun, Uttarakhand.
- 3 years of experience as an Assistant professor in Women Institute of Technology, Govt. Institute, Dehradun, Uttarakhand (From Dec 2014 to Dec 2017).

Research Publications :

1. **Aakanksha Devrari,** Adesh Kumar "Chip Design and FPGA Device Analysis of Turbo Encoder and Decoder for Communication System", International Journal of Reconfigurable and Embedded Systems IJRES), Vol. 12, No. 2, July 2023, pp. 174-185, DOI: http://doi.org/10.11591/ijres.v12.i2.pp174-185. **(Published) Scopus Indexed.**
2. **Aakanksha Devrari,** Adesh Kumar "Reconfigurable Linear Feedback Shift register for Wireless Communication", International Journal of Reconfigurable and Embedded Systems (IJRES), Vol. 12, No. 2, July 2023, pp. 195-204, DOI: http://doi.org/10.11591/ijres.v12.i2.pp195-204 **(Published) Scopus Indexed.**
3. **Aakanksha Devrari**, Adesh Kumar, Piyush Kuchhal "Global Aspects and Overview of 5G Multimedia Communication", Multimedia Tools and Applications, Springer (**Published), (SCI Indexed, Impact Factor = 3.6)**
4. Adesh Kumar, Kamal Bansal, Deepak Kumar, **Aakanksha Devrari**, Roushan Kumar, Prashant Mani, "FPGA Applications of Power Plant Monitoring", Nuclear Engineering & Technology, Elsevier, 2021, Vol. 53, No. 7, pp(1167-1175), Doi: https://doi.org/10.1016/j.net.2020.09.003**, Published, SCI Indexed.**
5. Amit Kumar, Adesh Kumar, **Aakanksha Devrari** "Hardware chip performance analysis of different FFT architecture", International Journal of Electronics (TETN), Ta

ylor & Francis. Doi: https://doi.org/10.1080/00207217.2020.1819441, **Published, S CI Indexed.**

6. **Aakanksha Devrari**, Adesh Kumar, Himanshu Chauhan, Amit Kumar "Design an d FPGA Implementation of LDPC Decoder Chip for Communication System using VHDL", International Journal of Recent Technology and Engineering (IJRTE), Vo lume-8, Issue-2, July 2019, pp(2526-2532), **Published, Scopus Indexed.**
7. Amit Kumar, Adesh Kumar, Manish Pandey and **Aakanksha Devrari** "Design and Implementation of Memory Based Pipelined FFT Architecture for Complex Valued Signals", Journal of Engineering and Applied Sciences", Dubai, UAE, Vol.12, Issu e 12, 2017, **Published, Scopus Indexed.**
8. Adesh Kumar, Pavan Chauda, **Aakanksha Devrari** "Machine Learning Approach f or Brain Tumor Detection and Segmentation", International Journal of Organization al and Collective Intelligence, IGI Global, 2021, Vol.11, No.3, **Published, ACM D igital Library, IET Inspecs.**
9. Shraddha Singh, Adesh Kumar, **Aakanksha Devrari** & Amit Kumar "ASIC Imple mentation of Programmable Timer Subsystems for WSN-SOC with wishbone Arch itecture on a Single Chip", National Academy Science Letters, pp. 231–234, 2022, DOI: https://doi.org/10.1007/s40009-022-01112-y, **Published, SCI Indexed**.
10. Manish Bansal, Amit Kumar, **Aakanksha Devrari**, Abhinav Bhat "Implementation Of Modular Exponentiation Using Montgomery Algorithms", International Journal of Scientific & Engineering Research, Volume 6, Issue 11, November-2015, ISSN 2229-5518, **Published**.
11. **Aakanksha Devrari**, Adesh Kumar, Shraddha Singh, Amit Kumar "Design and Im plementation of MAC Protocol based CDMA system for solving Near Far Effect us ing VHDL", International Journal of Scientific & Engineering Research, Volume 5, Issue 7, July-2014, pp(974-978), **Published, Indexed in Thomson Reuters.**
12. Shraddha Singh, Adesh Kumar, **Aakanksha Devrari**, Amit Kumar "Design of Adv anced Microprocessor Bus Architecture (AMBA) with Arbitration Scheme for AR M Processor using VHDL", International Journal of Electronics & Communication Technology (IJECT)-Vol 5, 2014, **Published**.
13. Abhinav Bhat, Amit Kumar, **Aakanksha Devrari**, Manish Bansal "VHDL Design and Synthesis of PCI Express Bus Controller", International Journal of Scientific &

Engineering Research, Volume 6, Issue 11, November-2015, ISSN 2229-5518, **Published.**

Workshops/ Webinar/FDP:

1. Webinar on Job Simulator organized by MIMT, Greater Noida, U.P.
2. Webinar on "Beyond the Boundaries: Reinventing Horizons" organized by Swami Keshvanand Institute of Technology, Jaipur.
3. Webinar on "Expand your Resources for Remote learners with IEEE eLearning library, UPES, Dehradun, Uttarakhand.
4. Webinar on "Effective E- Learning Resource Creation" organised by KLE college of Pharmacy, Vidyanagar, Hubli.
5. Online Scientific writing Program on "Structuring your Manuscript to impress Journal Editors and Selecting a Journal", organized by Editage by CACTUS, in UPES, Dehradun, Uttarakhand.
6. One week FDP on "Nascent Methodologies, Challenges and Realms of Research" organized by DTU, Delhi.
7. National Webinar on "Stress Management" organised by FET, EK BHARAT SRESTH BHARAT cell, Gurukul Kangri Vishwavidhyalaya, Haridwa, Uttarakhand.
8. Webinar on "SAMAY KA MARM" Organised by FMS, Gurukul Kangri Vishwavidhyalaya, Haridwar, Uttarakhand.
9. Webinar on Research Opportunities by Prof. Santanu Ray, MD, Indian Institute of Metals, Kolkata organized by UPES, Dehradun, Uttarakhand.
10. National workshop on FPGA Prototyping using VHDL and Verilog Organized by DBIT, Dehradun, Uttarakhand.
11. Workshop on basic Matlab course from Ambic Institute of technology, Dehradun, Uttarakhand.
12. IEEE Workshop on Technology enabled teaching and learning in higher education organized at Graphic Era hill University, Dehradun,Uttarakhand.
13. IEEE Workshop on GaN devices and power amplifiers organized by IIT Roorkee.

Certification Courses

1. Understanding Research Methods
2. Machine Learning for All.

Books/ Chapters

1. Advances in Intelligent Systems and Computing, Proceeding of International Conference on Intelligent Communication, Control and Devices, "Design and FPGA Implementation of DSSS for Near Far Effect in MANET", Springer conference Ref . No. 45700, vol. 470, pp. (425-434), DOI. 10.1007/978-981-10-1708-7.

2. Advances in Intelligent Systems and Computing, Proceeding of International Conference on Intelligent Communication, Control and Devices, "Design and FPGA Implementation of 32 point FFT Processor", Springer conference Ref . No. 45700, vol. 479, pp. (285-292), DOI. 10.1007/978-981-10-1708-7

Conferences/Seminar

1. ICICCD- 2016 Presented Research paper entitled Design and FPGA Implementation of 32 point FFT Processor.
2. ICICCD-2016, Presented Research paper entitled Design and FPGA Implementation of DSSS for Near Far Effect in MANET.
3. Participated in All India seminar on brighter career through professional skills enhancement (SBCPSE-2015) Organized by Uttarakhand State Centre, IE(I), Dehradun.

Areas of Interest

1. Digital Communication
2. VLSI Technology
3. 5G communication

Technical Skills	
Programming	VHDL,VERILOG, Embedded C
Operating System	Windows (98/XP/Vista/7)
Tools/Platforms	**1.** Modelsim, **2.** Xilinx ISE 14.7, Xilinx Vivado, **3.** Spartan 3E FPGA, **4.** Virtex 5 FPGA, **5.** Zedboard Zynq-7000 Development Board **6.** TSPICE simulation software **7.** Keil C51 Development tool **8.** Proteus Design suite 8.0 for electronic design automation.

Professional Training	
Organization and Duration	**1.** Oil and Natural Gas Co-operation (ONGC), Dehradun, 6 weeks on "Study of Microwave Communication", Duration: 14.6.2010 to 30.7.2010 **2.** Instrument Research Development Establishment (I.R.D.E), Dehradun. on "Image Compression Using JPEG 2000 Discrete Wavelet Transform", Duration: 21.5.2013 to 16.7.2013.

Projects Details	
Project Title (B.Tech)	"Intelligence Traffic Control System using Zigbee Technology".
Organization	Uttaranchal Institute of Technology, Dehradun, Uttarakhand
Project description	It is mainly designed to ease the movement of vehicles that are having an emergency situation or high priority. The project is developed to control the traffic wirelessly with the help of 2.4 GHz communication system.
Thesis Title (M.Tech)	"VHDL implementation of a DS-CDMA MAC protocol for Ad-hoc networks".
Organization	Uttarakhand Technical University, Dehradun, Uttarakhand

Thesis Description	The Objective of this thesis is the implementation of MAC protocol system for solving Near-Far effect in Ad-hoc networks.

Strengths & Skills

1. Good Creative Skills.
2. Professional Attitude and Team Spirit
3. Determined to give best in any situation.

Personal Information:	
Residential Address	161/1/3A , Kochar colony(Officers Enclave), Jakhan, Rajpur road, Dehradun
Father's Name	Jagdish Chandra Devrari
Date of Birth	08-08-1990
Languages Known	English, Hindi

Reference: Dr. Adesh Kumar, Senior Associate Professor, Electrical Department, School of Engineering, UPES, Dehradun.

Declaration:

I consider myself familiar with Electronics & communication Aspects. I am also confident of my ability to work in a team.

I hereby declare that the information furnished above is true to the best of my knowledge.

(AAKANKSHA DEVRARI)